AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An apparatus for processing data, said apparatus comprising:

data processing logic operable to perform data processing operations; and

an instruction decoder operable to decode program instructions specifying data processing operations to be performed by said data processing logic and to control said data processing logic to perform said data processing operations; wherein

said instruction decoder is operable in a first mode in which program instructions of a first instruction set are decoded and in a second mode in which program instructions of a second instruction set are decoded, a subset of program instructions of said first instruction set having a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for storage order differences, all bits are identical and forming a common subset of instructions representing at least one class of instructions, said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode.

2. (Previously Presented) The apparatus as claimed in claim 1, wherein said instruction decoder is operable to use common portions of said data processing logic to execute instructions of said common subset of instructions.

3. (Previously Presented) The apparatus as claimed in claim 1, wherein said common subset of instructions includes a class of instructions being coprocessor instructions operable to control coprocessor data processing operations using coprocessor logic common to said first instruction set and said second instruction set.

4. (Previously Presented) The apparatus as claimed in claim 3, wherein all unconditional coprocessor instructions are within said common subset.

5. (Presently Presented) The apparatus as claimed in claim 1, wherein said first instruction set is a fixed length instruction set of N-bit instructions.

6. (Previously Presented) The apparatus as claimed in claim 5, wherein N is one of 32 or 16.

7. (Previously Presented) The apparatus as claimed in claim 1, wherein said second instruction set is a variable length instruction set.

8. (Previously Presented) The apparatus as claimed in claim 1, wherein at least one program instruction within said common subset of instructions performs common data processing operations in either said first mode or said second mode but generates different result data values depending upon whether said instruction decoder is operating in said first mode or said second mode.

9. (Previously Presented) The apparatus as claimed in claim 8, wherein said at least one program instruction generating different result data values includes a program counter value as an input operand.

10. (Previously Presented) The apparatus as claimed in claim 9, wherein a different relationship is maintained between said program counter value and an address of an instruction being executed depending upon whether said instruction decoder is operating in said first mode or said second mode.

11. (Previously Presented) The apparatus as claimed in claim 8, wherein said at least one program instruction generating different result data values includes a program status register value as an input operand.

12. (Currently Amended) A method of processing data, said method comprising the steps of:

performing data processing operations with data processing logic; and

decoding with an instruction decoder program instructions specifying data processing operations to be performed by said data processing logic and controlling said data processing logic to perform said data processing operations; wherein

in a first mode program instructions of a first instruction set are decoded and in a second mode program instructions of a second instruction set are decoded, a subset of program instructions of said first instruction set having a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating

for storage order differences, all bits are identical and forming a common subset of instructions representing at least one class of instructions, said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode.

13. (Previously Presented) The method as claimed in claim 12, wherein common portions of said data processing logic are used to execute instructions of said common subset of instructions.

14. (Previously Presented) The method as claimed in claim 12, wherein said common subset of instructions includes a class of instructions being coprocessor instructions operable to control coprocessor data processing operations using coprocessor logic common to said first instruction set and said second instruction set.

15. (Previously Presented) The method as claimed in claim 14, wherein all unconditional coprocessor instructions are within said common subset.

16. (Previously Presented) The method as claimed in claim 12, wherein said first instruction set is a fixed length instruction set of N-bit instructions.

17. (Previously Presentedd) The method as claimed in claim 16, wherein N is one of 32 or 16.

18. (Previously Presented) The method as claimed in claim 12, wherein said second instruction set is a variable length instruction set.

19. (Previously Presented) The method as claimed in claim 12, wherein at least one program instruction within said common subset of instructions performs common data processing operations in either said first mode or said second mode but generates different result data values depending upon whether said instruction decoder is operating in said first mode or said second mode.

20. (Previously Presented) The method as claimed in claim 19, wherein said at least one program instruction generating different result data values includes a program counter value as an input operand.

21. (Previously Presented) The method as claimed in claim 20, wherein a different relationship is maintained between said program counter value and an address of an instruction being executed depending upon whether said instruction decoder is operating in said first mode or said second mode.

22. (Previously Presented) The method as claimed in claim 19, wherein said at least one program instruction generating different result data values includes a program status register value as an input operand.

23. (Currently Amended) A computer program product embodied in a storage medium for storing a computer program operable to control a data processing apparatus containing data processing logic operable to perform data processing operations, said computer program comprising:

program instructions of a first instruction set and program instructions of a second instruction set, that control said data processing logic to perform said data processing operations; wherein

a subset of program instructions of said first instruction set have a common storage order compensated encoding with a subset of program instructions of said second instruction set and such that, after compensating for storage order differences, all bits are identical form a common subset of instructions representing at least one class of instructions, said common subset of instructions controlling data processing logic to perform the same data processing operations independent of whether instructions of said first instruction set or of said second instruction set are being decoded.

24. (Previously Presented) The computer program product as claimed in claim 23, wherein common portions of said data processing logic are used to execute instructions of said common subset of instructions.

25. (Previously Presented) The computer program product as claimed in claim 23, wherein said common subset of instructions includes a class of instructions being coprocessor instructions operable to control coprocessor data processing operations using coprocessor logic common to said first instruction set and said second instruction set.

26. (Previously Presented) The computer program product as claimed in claim 25, wherein all unconditional coprocessor instructions are within said common subset.

27. (Previously Presented) The computer program product as claimed in claim 23, wherein said first instruction set is a fixed length instruction set of N-bit instructions.

28. (Previously Presented) The computer program product as claimed in claim 27, wherein N is one of 32 or 16.

29. (Previously Presented) The computer program product as claimed in claim 23, wherein said second instruction set is a variable length instruction set.

30. (Previously Presented) The computer program product as claimed in claim 23, wherein at least one program instruction within said common subset of instructions performs common data processing operations when instructions of either said first instruction set or said second instruction set are being decoded but generates different result data values.

31. (Previously Presented) The computer program product as claimed in claim 30, wherein said at least one program instruction generating different result data values includes a program counter value as an input operand.

32. (Previously Presented) The computer program product as claimed in claim 31, wherein a different relationship is maintained between said program counter value and an address of an instruction being executed depending upon whether said instruction decoder is operating in said first mode or said second mode.

33. (Previously Presented) The computer program product as claimed in claim 30, wherein said at least one program instruction generating different result data values includes a program status register value as an input operand.